



正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP6212A

REVISION : 2.1

DATE : Jun. 16th, 2021

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		

正基科技股份有限公司



AP6212A Data Sheet

Address:

8F, No.15-1 Zhonghua Road, Hsinchu Industrial Park, Hukou,
Hsinchu, Taiwan, 30352
<http://www.ampak.com.tw>

Revision History

Date	Revision Content	Revised By	Version
2015/06/06	- Initial Release	Brian	1.0
2016/03/11	- Add Reflow Suggestion and MLS	Beth	1.1
2016/06/20	- Modify Pin Definition -Change storage & operation Temp. Range - Humidity	Richard	1.2
2017/03/13	- Modify BT Spec	Richard	1.3
2017/09/06	- Modify Recommended Reflow Profile	Richard	1.4
2017/12/08	- Modify WLAN RF Spec	Richard	1.5
2018/11/27	-Modify Wi-Fi support channel. -Modify General Specification.	Richard	1.6
2020/04/24	-Update Form -Modify Package Information	Richard	1.7
2021/01/13	-Update BT specification	Richard	1.8
2021/02/23	-Update Block Diagram	Richard	1.9
2021/05/07	-Update Wi-Fi Sensitivity Specification	Richard	2.0
2021/06/16	-Modify VBAT and VDDIO supply voltage Specification	Richard	2.1

Contents

1. Introduction	3
2. Features	4
3. Deliverables	5
3.1 Deliverables	5
3.2 Regulatory certifications	5
4. General Specification	6
4.1 General Specification	6
4.2 Voltages	6
4.2.1 Absolute Maximum Ratings	6
4.2.2 Recommended Operating Rating	6
5. WiFi RF Specification	7
5.1 2.4GHz RF Specification	7
6. Bluetooth Specification	9
6.1 Bluetooth Specification	9
7. FM Specification	10
7.1 FM Specification	10
8. Pin Assignments	11
8.1 Pin Outline	11
8.2 Pin Definition	11
9. Dimensions	13
9.1 Physical Dimensions	13
9.2 Layout Recommendation	14
10. External clock reference	15
10.1 SDIO Pin Description	16
11. Host Interface Timing Diagram	17
11.1 Power-up Sequence Timing Diagram	17
11.2 SDIO Default Mode Timing Diagram	19
11.3 SDIO High Speed Mode Timing Diagram	20
12. Recommended Reflow Profile	21
13. Package Information	22
13.1 Label	22
13.2 Dimension	23
13.3 MSL Level / Storage Condition	25

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

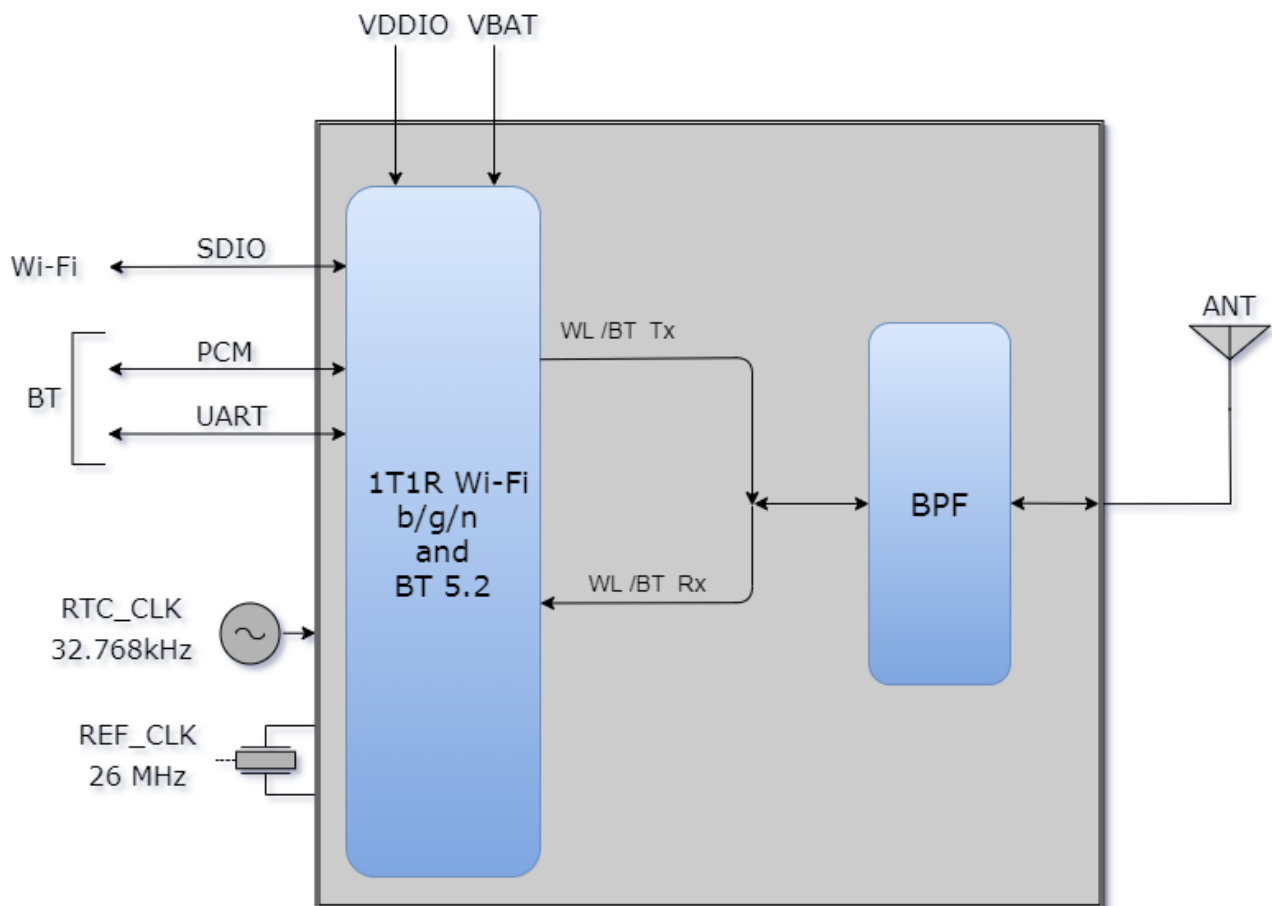
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / I2S / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V5.2 with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
 - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
 - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6212A
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
WiFi Interface	SDIO V2.0
BT Interface	UART / PCM
Operating temperature ^{a,b}	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

- a. The operating temperature 65 to 85°C is feasible at conditional environment. Please examine the reliability on final product.
- b. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for -10°C to 55°C and 3.2V < VBAT < 3.8V.

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	+5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	+3.8	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.71	1.8	1.98	V
	2.97	3.3	3.63	V

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch13
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm \pm 1.5dB @ EVM \leq -9dB
	802.11g /54Mbps : 15 dBm \pm 1.5dB @ EVM \leq -25dB
	802.11n /65Mbps : 14 dBm \pm 1.5dB @ EVM \leq -27dB
Sensitivity, tolerance \pm 2 dB CCK modulation PER \leq 8% 、 OFDM modulation PER \leq 10%	
802.11n_20MHz	- MCS=0 PER @ -88 dBm,
	- MCS=1 PER @ -87 dBm,
	- MCS=2 PER @ -86 dBm,
	- MCS=3 PER @ -84 dBm,
	- MCS=4 PER @ -81 dBm,
	- MCS=5 PER @ -77 dBm,
	- MCS=6 PER @ -75 dBm,
	- MCS=7 PER @ -72 dBm,
802.11g	- 6Mbps PER @ -90 dBm,
	- 9Mbps PER @ -90 dBm,
	- 12Mbps PER @ -88 dBm,
	- 18Mbps PER @ -86 dBm,
	- 24Mbps PER @ -83 dBm,
	- 36Mbps PER @ -80 dBm,
	- 48Mbps PER @ -77 dBm,
	- 54Mbps PER @ -75 dBm,
802.11b	- 1Mbps PER @ -95 dBm,
	- 2Mbps PER @ -94 dBm,
	- 5.5Mbps PER @ -92 dBm,

	- 11Mbps PER @ -88 dBm,
Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	BDR(1Mbps) 、 EDR(2 、 3Mbps) 、 LE(1Mbps)		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402MHz ~ 2480MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK		
RF Specification			
	Min.	Typical.	Max.
Output Power¹		5	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-87 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-85 dBm	
Sensitivity @ PER=30.8% for LE		-86 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

NOTE¹ : Output power can be configured by HCD firmware.

7. FM Specification

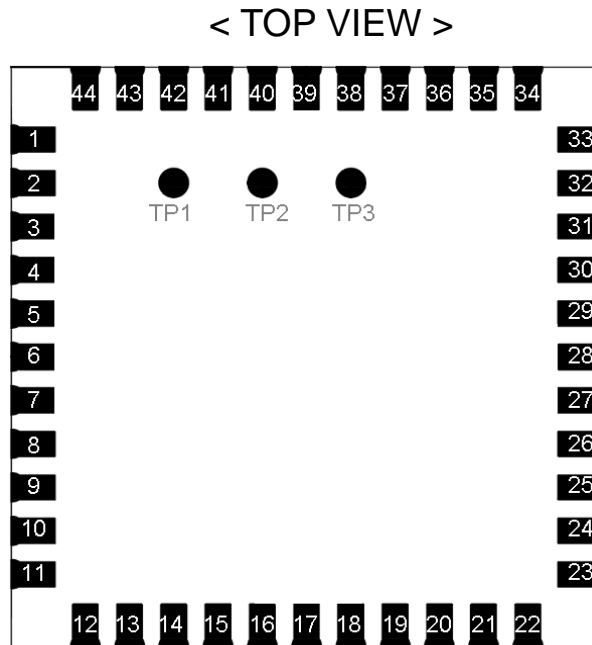
7.1 FM Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description				
General Specification					
Frequency Band	65MHz-108MHz				
Host Interface	HCI UART, I2S/PCM				
Frequency step	Minimum 10 KHz				
Analog Audio output load	$R_L > 30K\Omega$, $C_L > 20pF$				
Characteristics	Condition	MIN	TYP	MAX	UNIT
Receiver Spec.	FM only, Sensitivity, $SNR \geq 26dB$		-5		dBuV
	Audio harmonic distortion, mono ($V_{in}=2mV$ EMF, $\Delta f=75KHz$)	fmod=1KHz		0.8	%
		fmod=3KHz		0.8	
	Maximum SNR (fmod=1KHz, $\Delta f=22.5KHz$, BW=300Hz to 15KHz)	mono		69	dB
		Stereo		64	
Maximum input level, SNR > 26dB				107	dBuV

8. Pin Assignments

8.1 Pin Outline



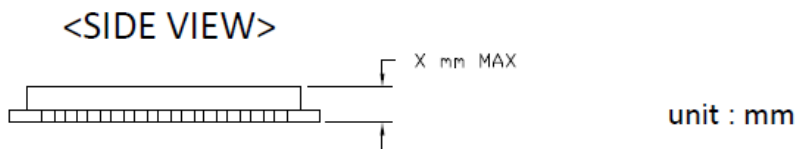
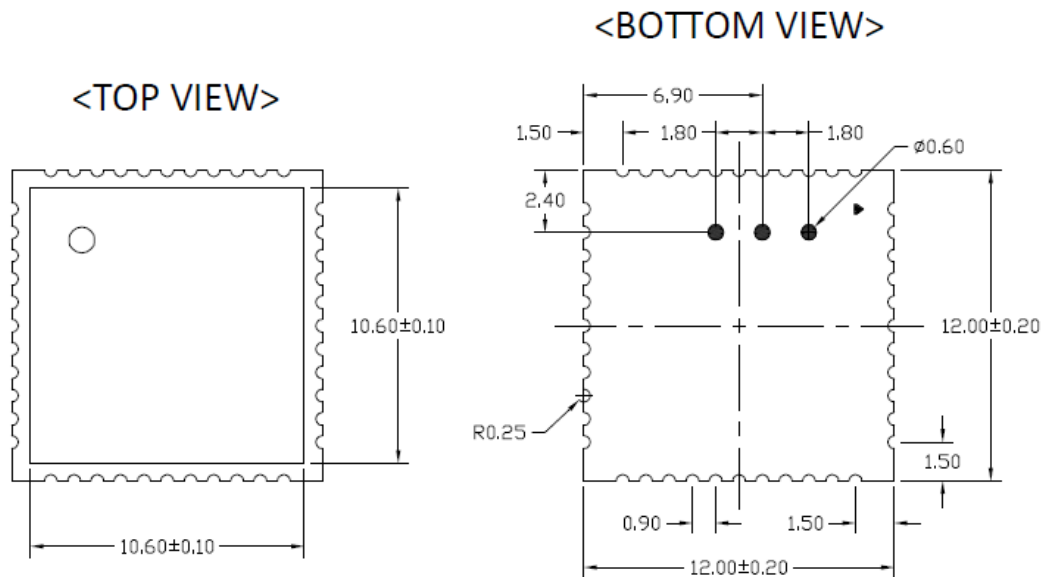
8.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	FM_RX	I	FM radio RF input antenna port
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	CLK_REQ	O	The AP6212A asserts CLK_REQ when Bluetooth, or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the AP6212A powers up or resets when VDDIO is present.
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input

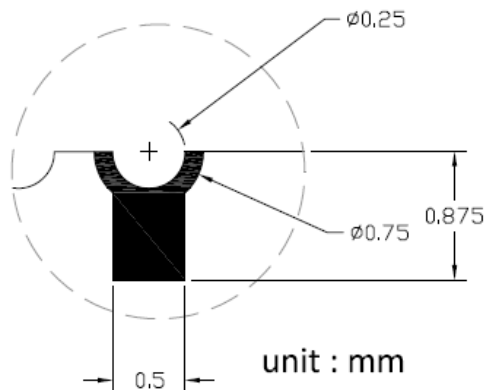
11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	GPIO2	I/O	WL_GPIO2
40	GPIO1	I/O	WL_GPIO1
41	UART_RTS_N	O	Bluetooth/FM UART interface
42	UART_TXD	O	Bluetooth/FM UART interface
43	UART_RXD	I	Bluetooth/FM UART interface
44	UART_CTS_N	I	Bluetooth/FM UART interface
45	TP1	O	FM Analog AUDIO left output
46	TP2	O	FM Analog AUDIO right output
47	TP3 (NC)	—	Floating (Don't connected to ground)

9. Dimensions

9.1 Physical Dimensions



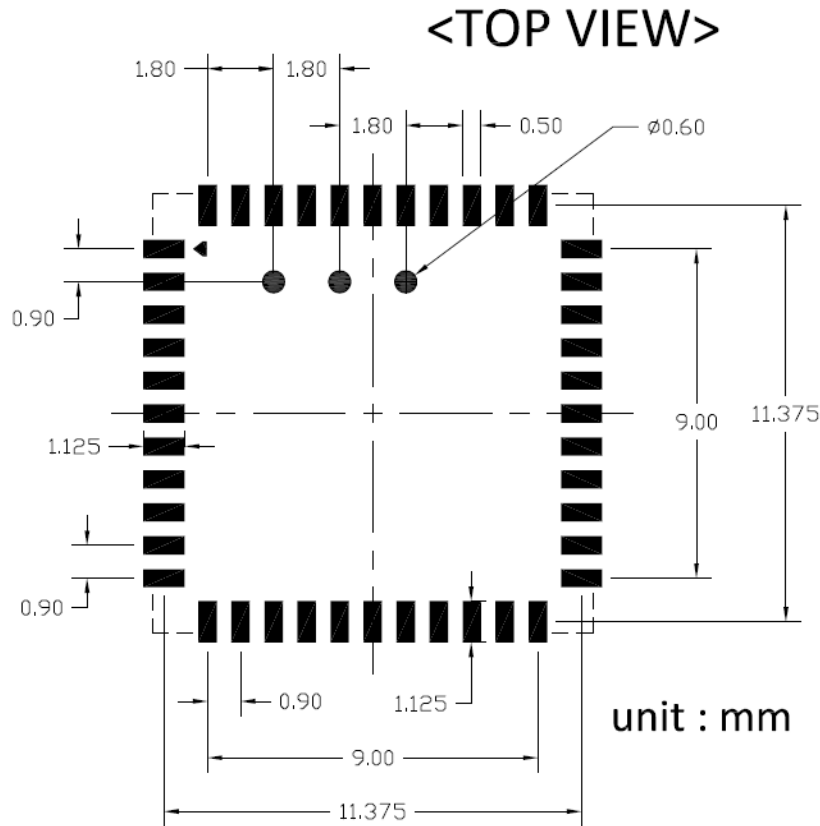
X=1.6mm



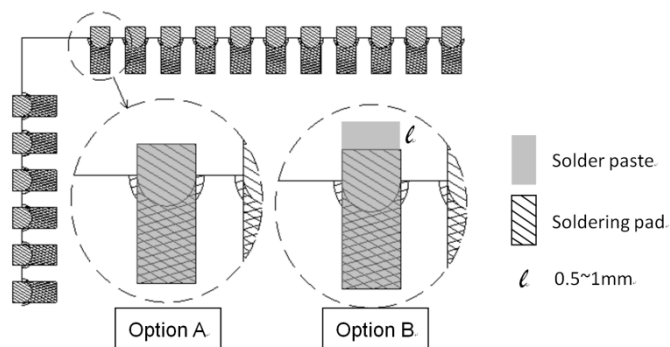
Detail A

9.2 Layout Recommendation

(Unit: mm)



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).



10. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Module input Signal Level	400~3300	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

External Ref_CLK signal characteristics

No.	Item	Symb.	Electrical Specification				Remark
			Min.	Type	Max.	Units	
1	Nominal Frequency	F0	26.00000			MHz	
2	Mode of Vibration		Fundamental				
3	Frequency Tolerance	$\Delta F/F0$	-10	-	10	ppm	at 25°C±3°C
4	Operating Temperature Range	T _{OPR}	-30	-	85	°C	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T _{STG}	-55	-	125	°C	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V _{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

10.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

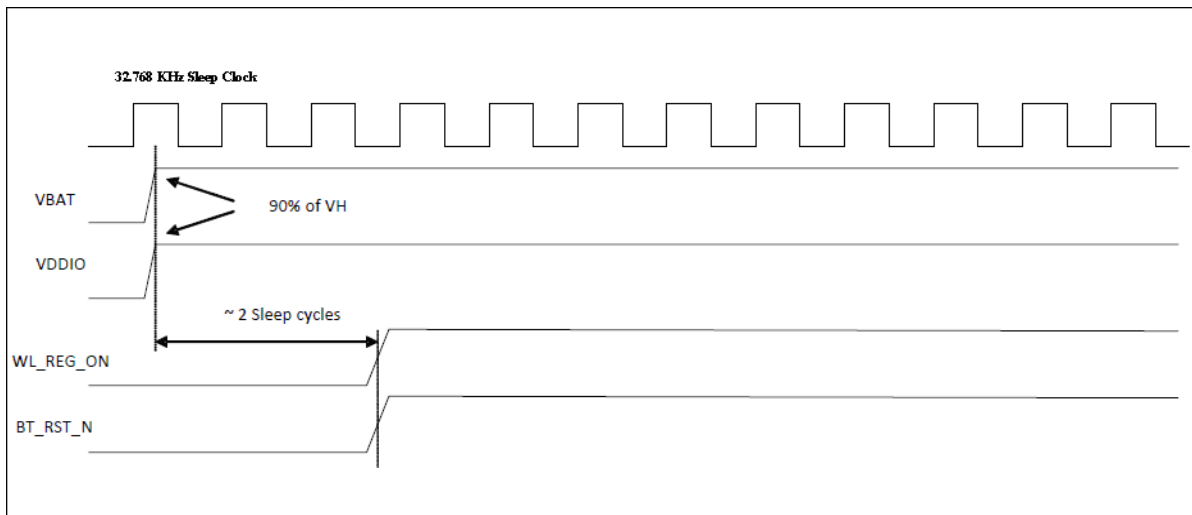
11. Host Interface Timing Diagram

11.1 Power-up Sequence Timing Diagram

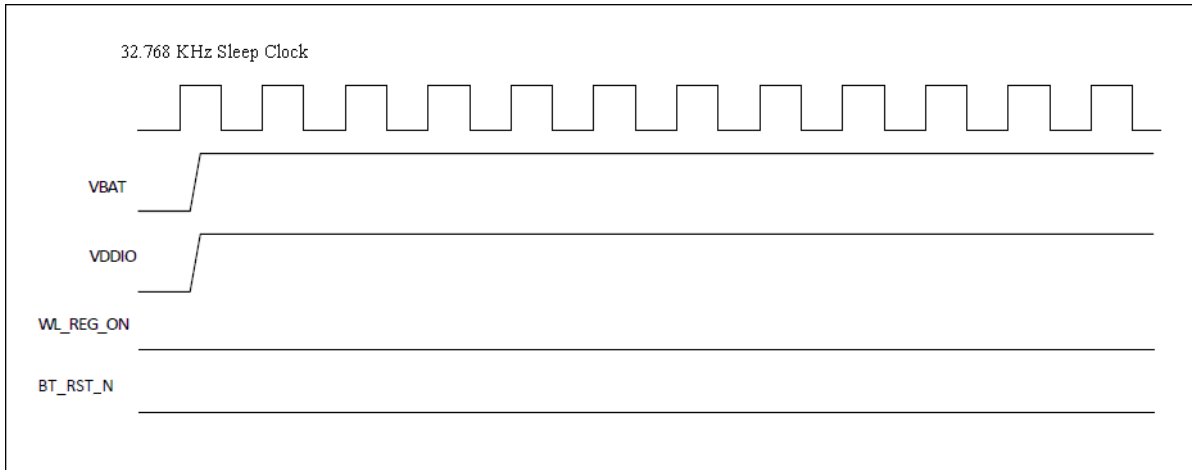
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

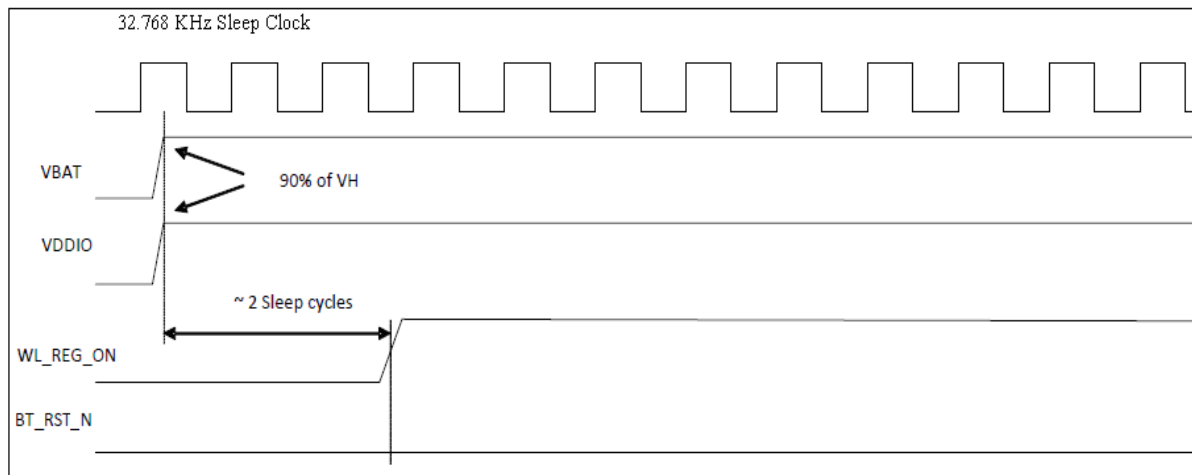
- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT_RST_N: Low asserting reset for Bluetooth and FM only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



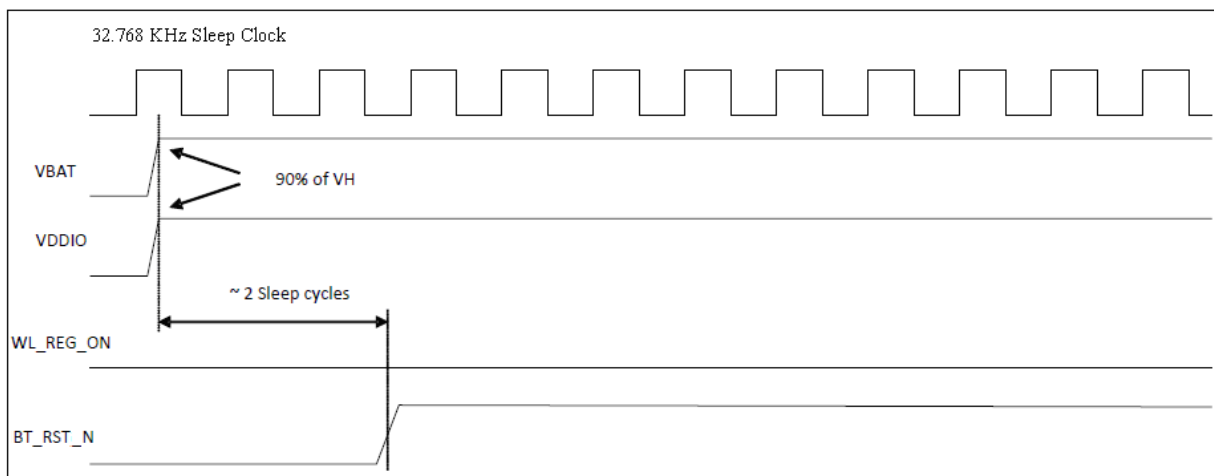
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

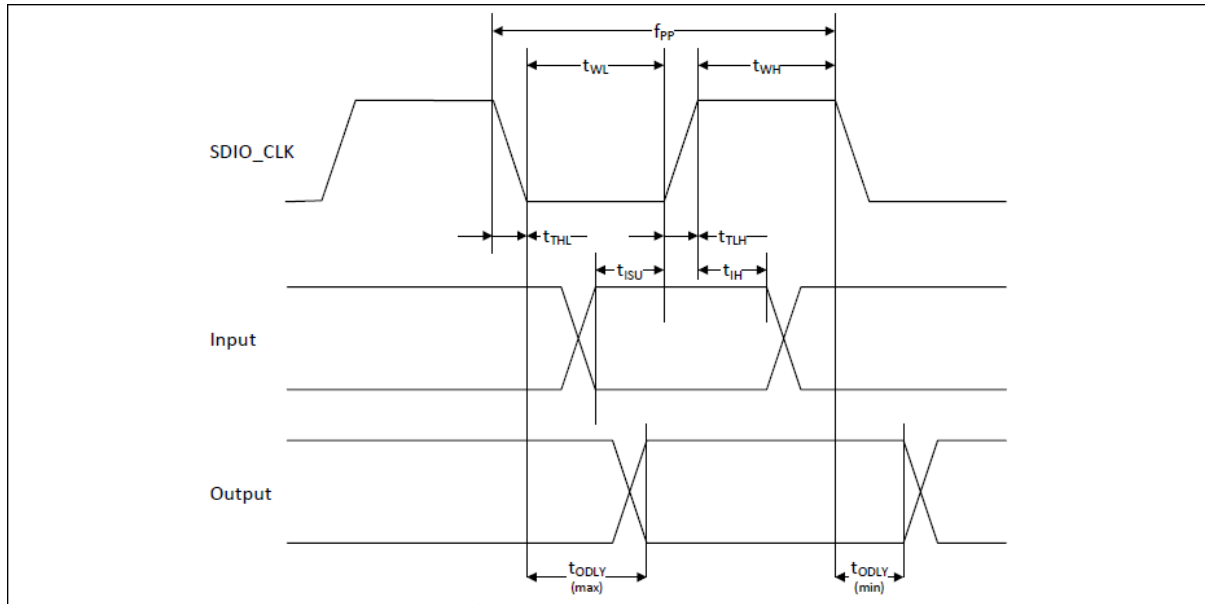


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

11.2 SDIO Default Mode Timing Diagram

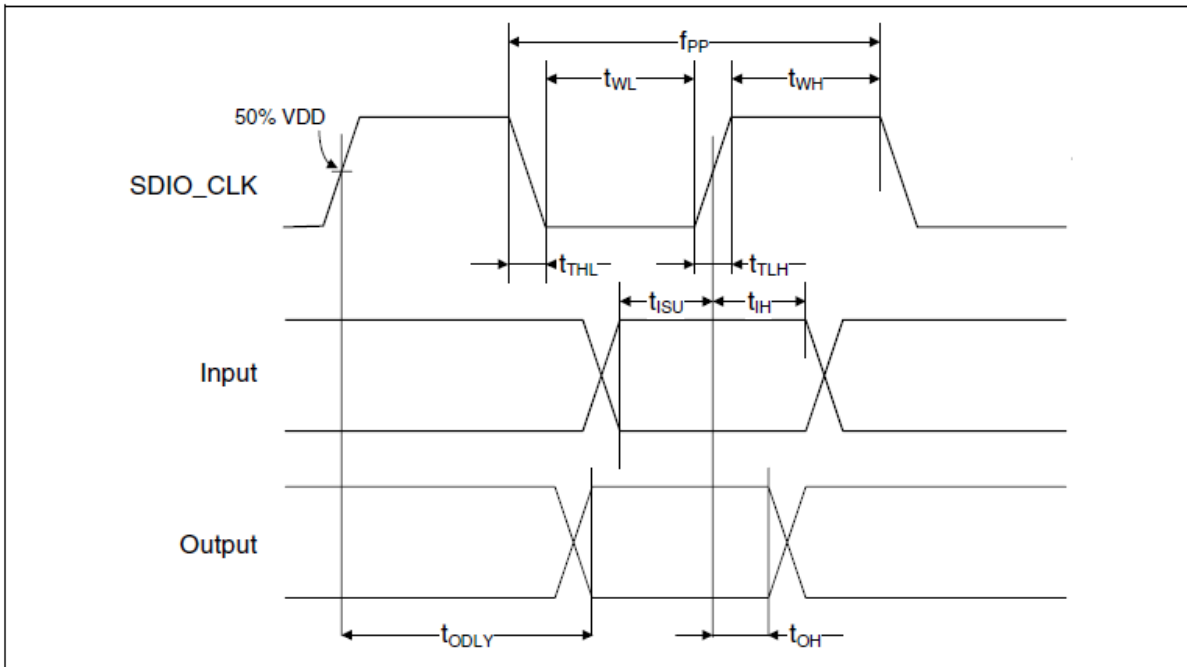


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency-Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock low time	t_{THL}	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time - Identification mode	t_{ODLY}	0	-	50	ns

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. $\min(V_{ih}) = 0.7 \times V_{DDIO}$ and $\max(V_{il}) = 0.2 \times V_{DDIO}$.

11.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	f _{PP}	0	-	50	MHz
Frequency-Identification mode	f _{OD}	0	-	400	kHz
Clock low time	t _{WL}	7	-	-	ns
Clock high time	t _{WH}	7	-	-	ns
Clock rise time	t _{TLH}	-	-	3	ns
Clock low time	t _{THL}	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t _{ISU}	6	-	-	ns
Input hold time	t _{IH}	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t _{ODLY}	-	-	14	ns
Output hold time	t _{OH}	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

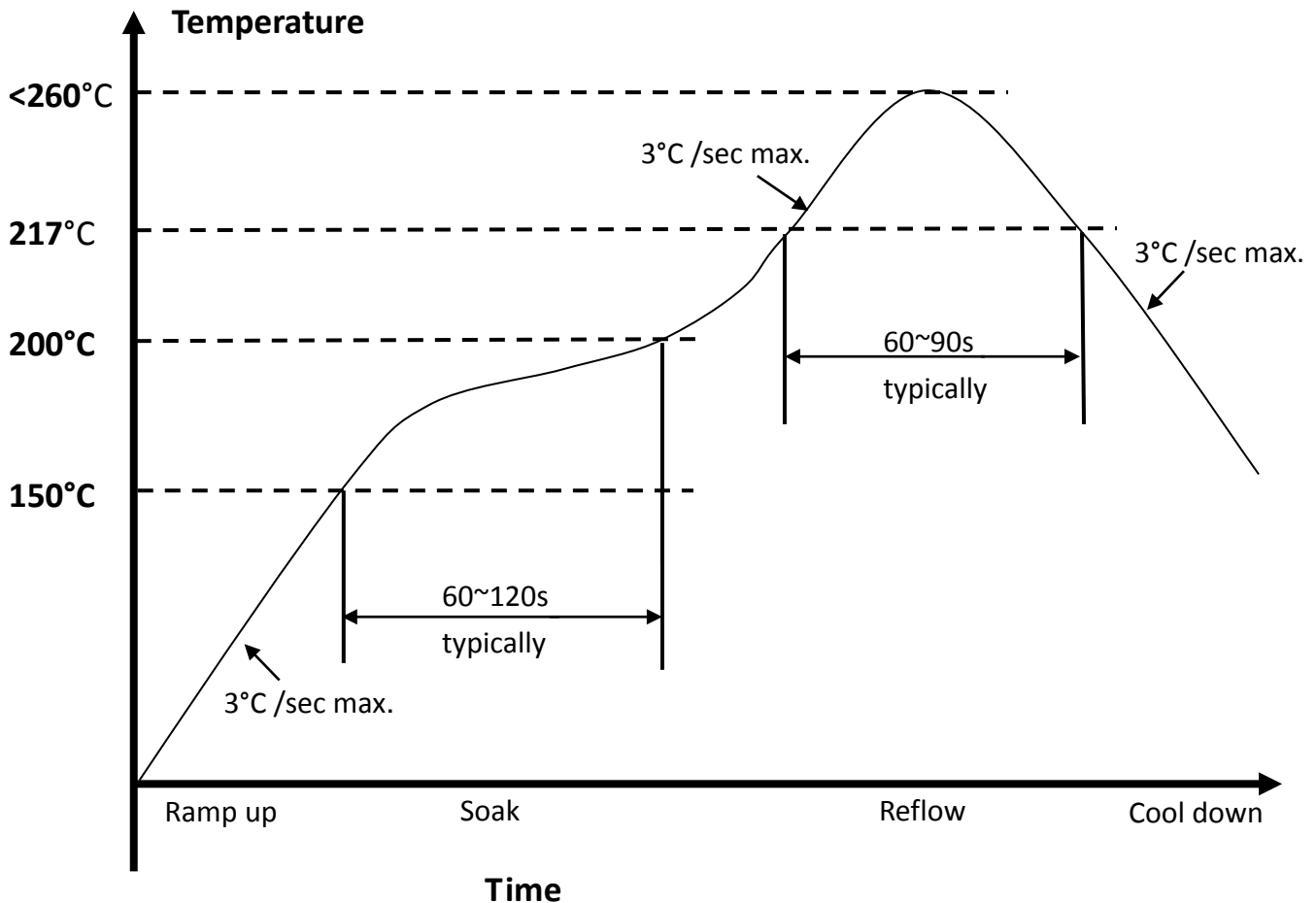
b. min(V_{Ih}) = 0.7 x V_{DDIO} and max(V_{Iil}) = 0.2 x V_{DDIO}.

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <math><250^{\circ}\text{C}</math>

Number of Times : ≤ 2 times



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <math><260^{\circ}\text{C}</math>
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component


13. Package Information

13.1 Label








Label A → Anti-static and humidity notice









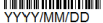
Label B → MSL caution / Storage Condition

	Caution	LEVEL
	This bag contains MOISTURE-SENSITIVE DEVICES	
		<input type="text"/> <small>If blank, see adjacent bar code label</small>
<ol style="list-style-type: none"> 1. Calculated shelf life in sealed bag: 12 months at <math>40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH) 2. Peak package body temperature: _____ $^{\circ}\text{C}$ <small>If blank, see adjacent bar code label</small> 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be <ol style="list-style-type: none"> a) Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small> b) Stored per J-STD-033 4. Devices require bake, before mounting, if: <ol style="list-style-type: none"> a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$ b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure 		
Bag Seal Date: _____		<small>If blank, see adjacent bar code label</small>
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

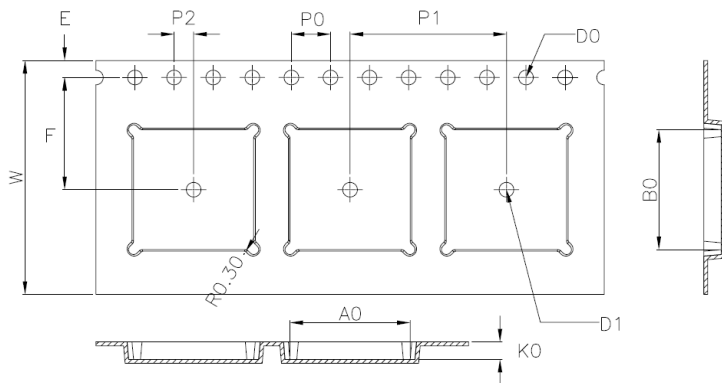
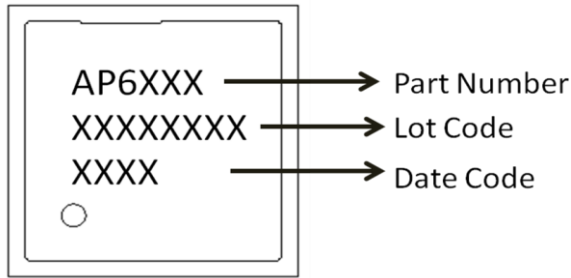
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	 9PKGYYMDDNNNNN
Model Name:	 APXXXXXXXX (R3HF)
P/N:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Date Code:	 YYWW
Lot Code:	 XXXXXXXXXX

Label D → Carton box label .

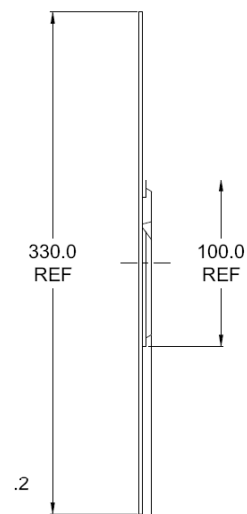
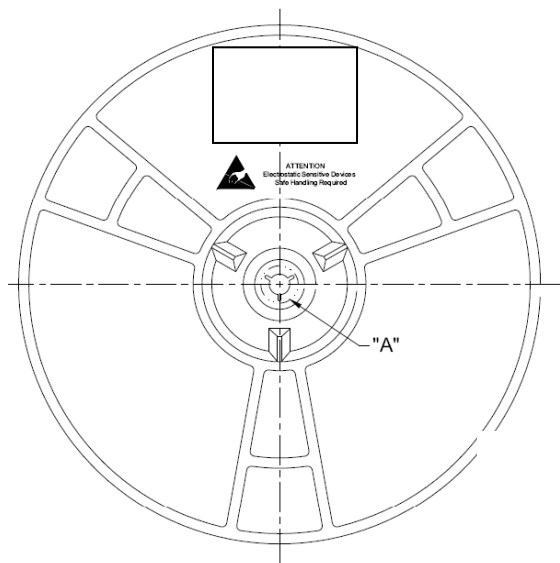
AMPAK Technology Inc.	
PO:	
AMK DEVICE:	
Model Name:	 APXXXXXXXX (R3HF)
Part No.:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Lot D/C:	 XXXXXXXXXX YYWW QQQQ
Manufacture:	 YYYY/MM/DD

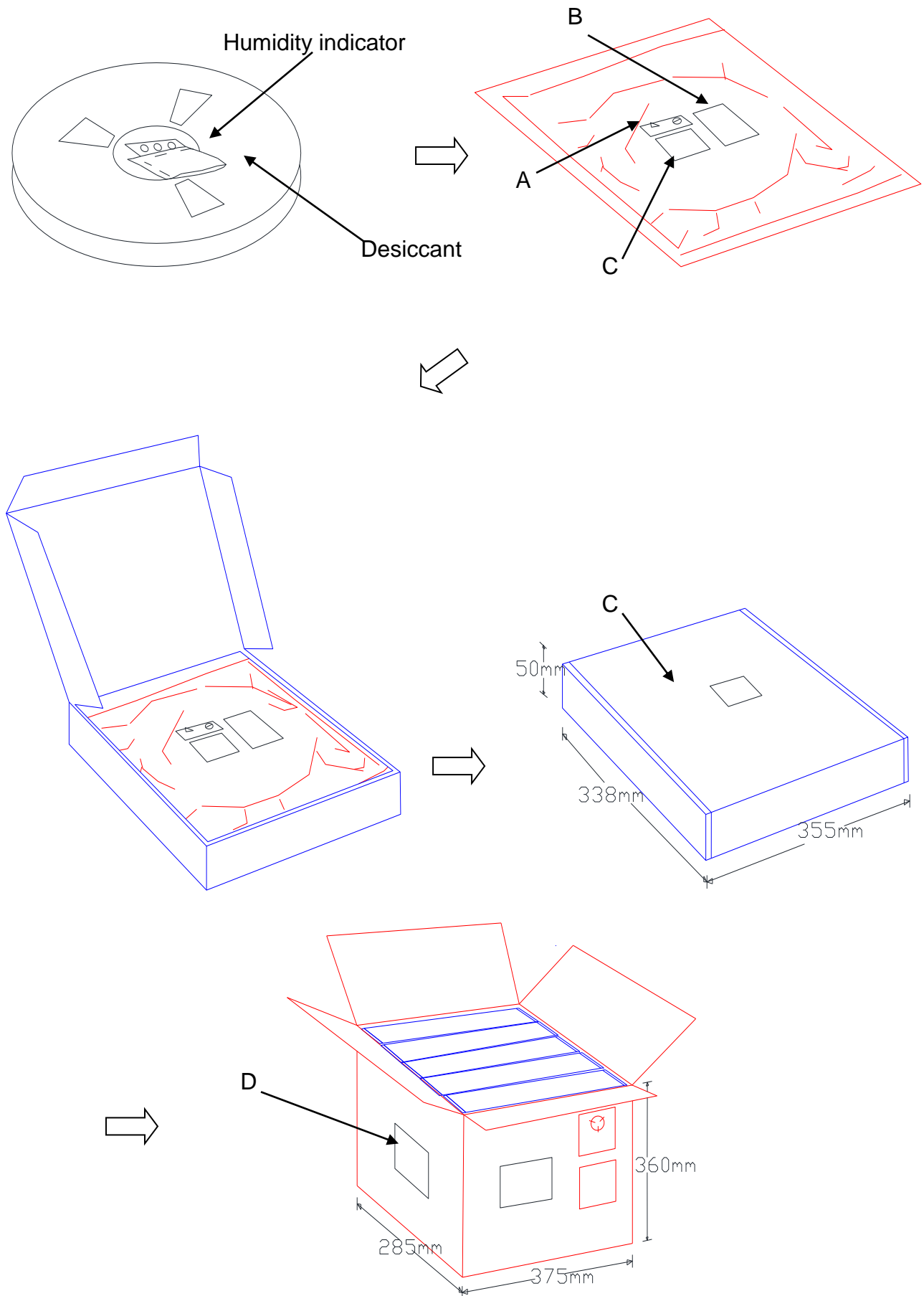
13.2 Dimension




W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 ^{+0.10} / _{-0.00}
D1	∅1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





13.3 MSL Level / Storage Condition

	<p>Caution This bag contains MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL 4 If blank, see adjacent bar code label</p>
<p>1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)</p> <p>2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label</p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p> <p>a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label $\leq 30^{\circ}\text{C} / 60\% \text{ RH}$, or</p> <p>b) Stored per J-STD-033</p> <p>4. Devices require bake, before mounting, if:</p> <p>a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$</p> <p>b) 3a or 3b are not met.</p> <p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</p>		
<p>Bag Seal Date: _____ If blank, see adjacent bar code label</p>		
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>		