PAC7673EE: Integrated Ambient Light and Proximity Sensor with I2C Interface

General Description:

PAC7673EE integrates both an ambient light sensor (ALS) and a proximity sensor (PS) with general I2C interface into a single chip.
The ambient light or proximity data can be accessed either periodically depending on the data integration period which is tunable from 50 ms to 8 s with minimal programmable step of 1.66 ms or by interrupt function when the data match the requirement of customized interrupt window. The PAC7673EE uses both a hardware pin and software bits to indicate an interrupt event has occurred. With the interrupt persist function, the interrupt occurs at once if the ALS or/and PS data meet the interrupt condition up to 16 times.

Key Features:

- Perfect human eye spectrum response
- General I2C interface up to 400 kbit/s with 4 different slave ID.
- Accurate lux readout under different circumstance light.
- Output code directly proportional to lux.
- 50 Hz/60 Hz de-flicker ability and IR rejection
- Detectable up to 24k lux with minimal resolution 1 Lux/code
- Built-in IR-LED switch
- PS data output
  - Continuous code through I2C bus
  - ON/OFF code through I2C bus or hardware pin.
- Ultra fast PS response (minimum report period is 1.66 ms) and high PS sensitivity.
- Ambient noise cancellation.

Applications:

- PAD Phone
- Tablet Personal Computer
- Automobile Application

Key Sensor Parameters:

Parameter	Value
Pixel Size (µm)	100x100µm^2
Report Rate	10Hz
Supply Voltage	2.5v~3.6v
Package Type	AIO 8L
Package Dimensions	3.94x2.36x1.35 mm^3

Ordering Information:

Part Number	Package Type
PAC7673EE	AIO 8L

Lead (Pb) Free RoHS 6 fully compliant

For any additional inquiries on ordering information, please contact us at sales@pixart.com

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1.0 System Level Description

1.1 Overview

For ambient light sensor (ALS) in PAC7673EE, it can detect ambient light illuminance with perfect human eye spectrum response. The detectable range is up to 24k Lux with minimal resolution 1 Lux/code with the great de-flicker ability which rejects 50 Hz/60H z flicker noise caused by common artificial fluorescent light sources.

For proximity sensor (PS) in PAC7673EE, the built-in LED switch controls an IR LED emitting IR light to a reflective target and the reflected IR intensity is sensed by high-IR-sensitivity photodiode, then converted to 8-bit proximity data. The noise light in circumstance is rejected by filtering and LED control. The conversion numbers and conversion time are all tunable.

The ambient light or proximity data can be accessed either periodically depending on the data integration period which is tunable from 50 ms to 8 s with minimal programmable step of 1.66 ms or by interrupt function when the data match the requirement of customized interrupt window. The PAC7673EE uses both a hardware pin and software bits to indicate an interrupt event has occurred. With the interrupt persist function, the interrupt occurs at once if the ALS or/and PS data meet the interrupt condition up to 16 times.

The PAC7673EE provide low operation current (103 µA operated at 2.8 V, 90 µA for sensor and circuit, 13 µA for IR LED with 100 mA ON peak current, 100 ms integration period) and ultra low suspend current (less than 0.5 µA).

1.2 Architecture Block Diagram

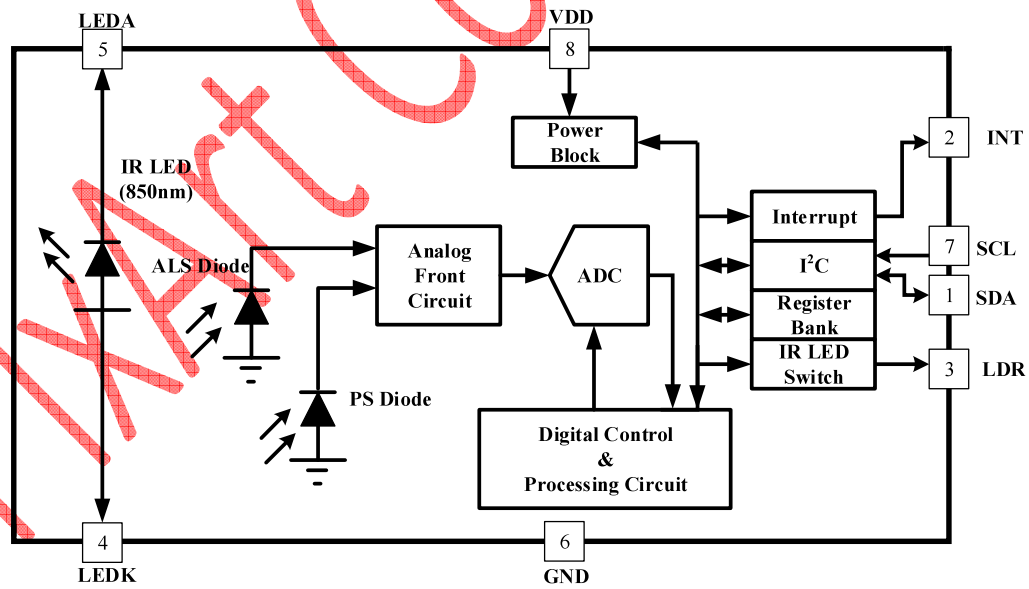

Figure 01. Architecture Block Diagram

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1.3 Signal Description

Signal	Description
SDA	I²C data pin
SCL	I²C clock pin
INT	Interrupt pin (Active low)
LDR	LED switch pin, connect to IR LED.
LEDK	LED cathode
LEDA	LED anode
VDD	Power supply
GND	Ground

Table 01. Signal Description

1.4 Pin Configuration

Pin NO.	Symbol	Type	Function
1	SDA	IN/OUT (Open Drain)	I²C data pin
2	INT	OUT (Open Drain)	Interrupt pin (Active low)
3	LDR	IN	LED switch pin, Connect to IR LED.
4	LEDK	OUT	LED cathode
5	LEDA	IN	LED anode
6	GND	GND	Ground
7	SCL	IN (Open Drain)	I²C clock pin
8	VDD	POWER	Power supply

Table 02. PAC7673EE Pin Configuration Table

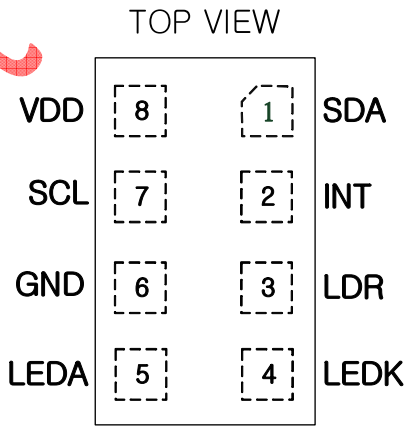

Figure 02. PAC7673EE Module Pin Configuration

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1.5 Reference Schematic

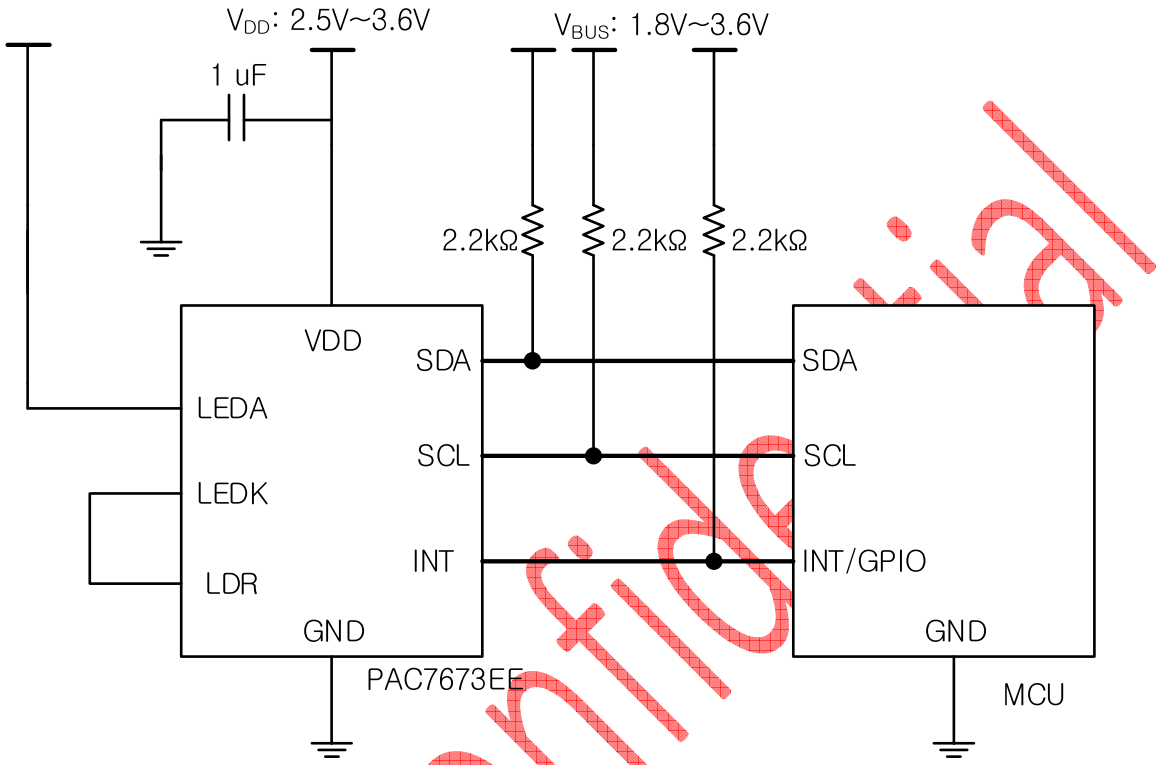

Figure 03. PAC7673EE Schematic

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1.6 Serial Interface Communication

i. I²C Timing Parameter

Parameter	Symbol	STANDARD MODE		FAST MODE		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency.	f_{scl}	10	100	10	400	kHz
Hold time for Start/Repeat Start. After this period, the first clock pulse is generated.	$t_{HD.STA}$	4		0.6		µs
Set-up time for a repeated Start.	$t_{SU.STA}$	4.7		0.6		µs
Low period of SCL clock.	t_{LOW}	4.7		1.3		µs
High period of SCL clock.	t_{HIGH}	4		0.6		µs
Data hold time.	$t_{HD.DAT}$	0		0		µs
Data set-up time.	$t_{SU.DAT}$	250		100		ns
Rise time of both SDA and SCL signals.	t_r		1000	-	300	ns
Fall time of both SDA and SCL signals.	t_f		300	-	300	ns
Set-up time for STOP condition.	$t_{SU.STO}$	4		0.6		µs
Bus free time between a STOP and START.	t_{BUF}	4.7		1.3		µs

** maximum current is 5mA and capacitance load spec. =100pF*

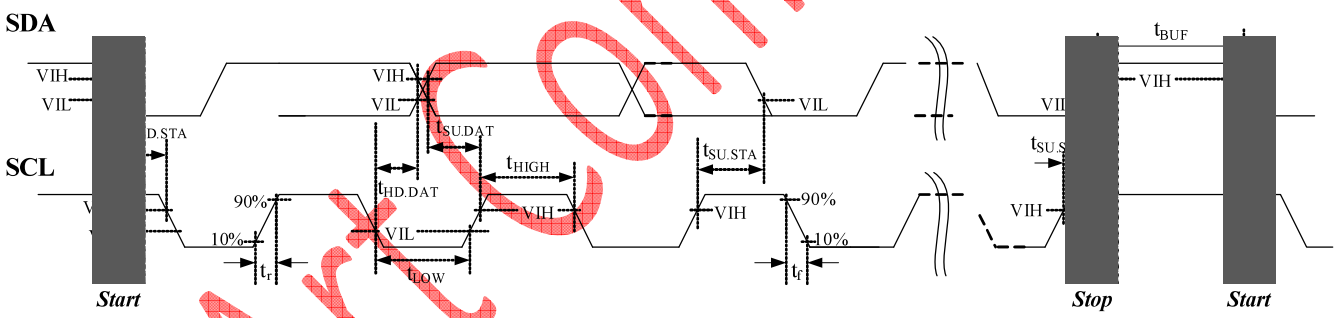

Figure 04. I²C Timing Diagram

ii. I²C General Description

I. SDA (serial data) and SCL (serial clock) form a two-wire serial interface compatible with I²C. The PAC7673EE is implemented as a slave-only device so it never drives SCL. It drives SDA during (host) read cycles and transmission of the Acknowledge bit. PAC7673EE uses 7-bit addressing and does not support clock stretching. The SDA and SCL pins are open-drain structure requiring external pull-up resistors.

II. Start and stop condition: SDA high to low transition while SCL is high defines a Start condition. SDA low to high transition while SCL is high defines a Stop condition. (Refer. to Figure 05)

III. Valid data: The data on SDA line must be stable during high period of SCL. MSB is always transferred first for each byte. LSB of the first byte is Read / Write control bit. (Refer. to Figure 06)

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IV. Both master and slave can transmit and receive data from the bus.

V. Acknowledge: The Receiving device should pull down SDA during high period of the 9th clock (SCL) after a complete byte has been received from the transmitter. In the case of the master receiving data from the slave, the master does not generate an Acknowledge bit after the last byte to indicate the end of a master read cycle.

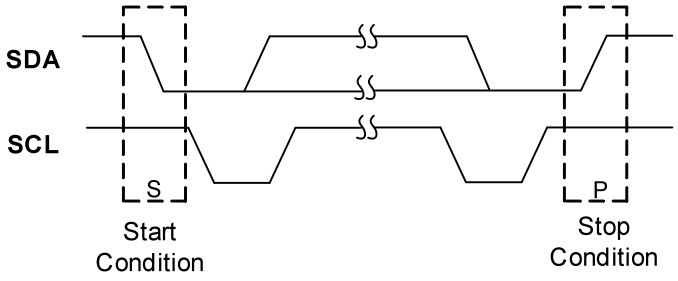


Figure 05. Start and Stop Conditions

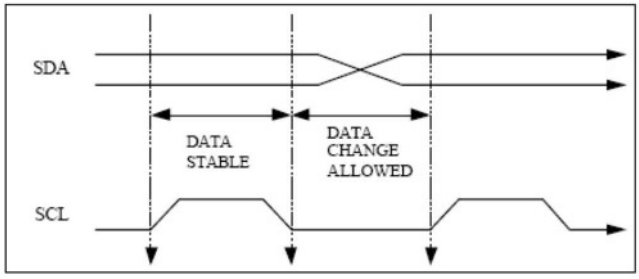
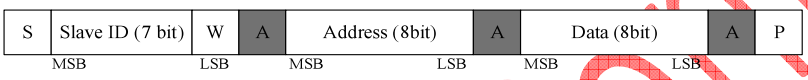


Figure 06. Valid Data

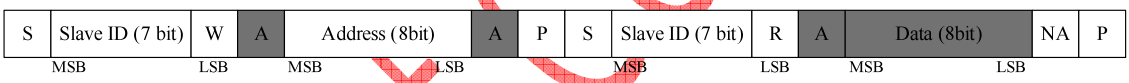
iii. I²C Protocol

The slave ID of PAC7673EE is **0x48** hex using 7 bit addressing protocol. Contact Pixart for other slave ID requirement.

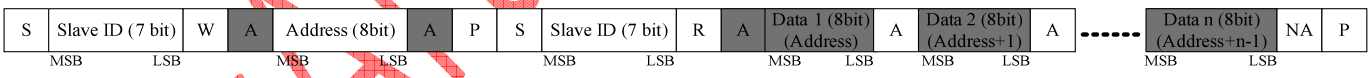
I. Single Write Protocol



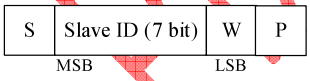
II. Single Read Protocol

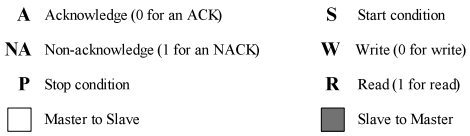


III. Burst Read Protocol



IV. I²C Wake-up command Protocol





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2.0 Operation Principle

2.1 Power-On Sequence

After power on, wait T_1 µs for PAC7673EE to stabilize and then write slave ID (0x48) to process I^2C wake-up. Then, The ALS/PS data can now be accessed through the I^2C bus.

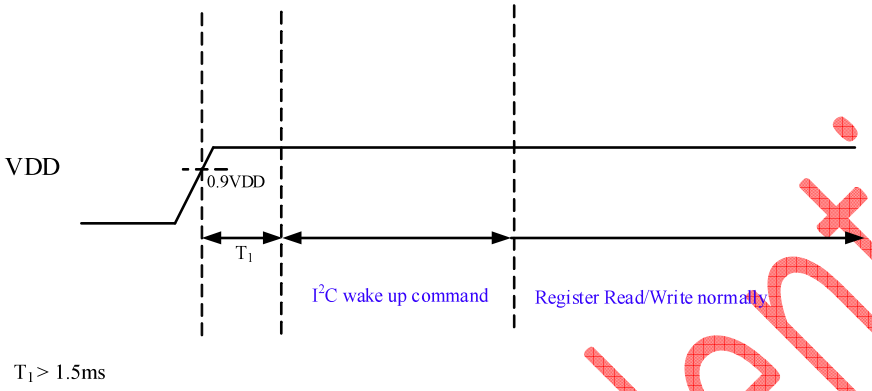

Figure 07. PAC7673EE Power-On Timing Diagram

2.2 State Machine

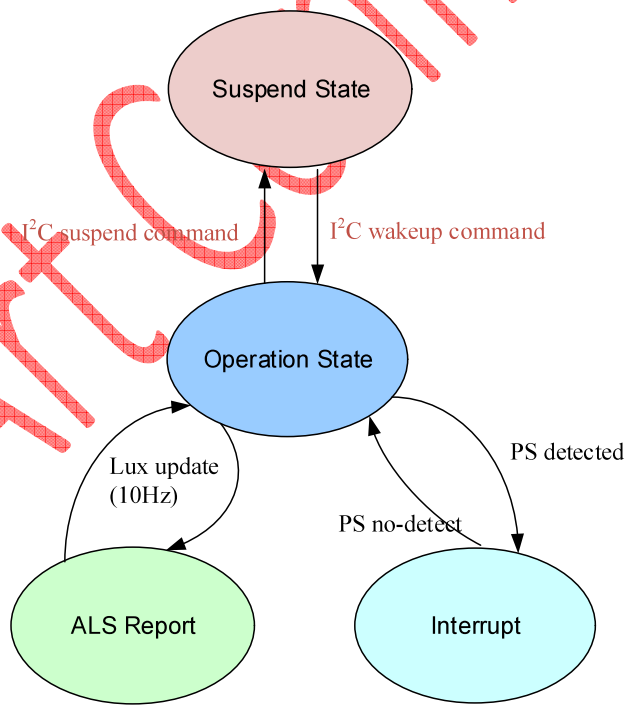

Figure 08. State Machine of ALS/PS Detection

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